ADM-SDEV-CFG2
User Manual

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1 Introduction

The **ADM-SDEV-CFG2** configuration module **board** forms part of the ADA-SDEV-KIT3/4 space FPGA development kit.

The ADM-SDEV-CFG2 board replaces the ADM-SDEV-CFG1 in this kit. These configuration boards connect to the configuration FMC socket of the ADM-SDEV-BASE board, allowing the Xilinx tools to interrogate and configure its FPGA.

The CFG2 is compatible with every model of Base board.

1.1 Key Features

Key Features

- Used in combination with the ADM-SDEV-BASE board
- Can be used in combination with the ADM-SDEV-FL1 QSPI flash daughter board (Supplied as standard)
- Alternatively, FPGA configuration signals are broken out onto this board.
- Single width FMC mezzanine card form factor
- Gigabit Ethernet PHY for communication with FPGA
- Serial port for RS-232 communication with FPGA
- 2x SATA sockets, allows access to 2 high speed serial lanes of the Base board FPGA
- IPASS Connector, allowing remote PCIe connection to the Base board FPGA
- Backwards compatible FMC pinout to Rev 1 Config board
- JTAG header which passes through to base board to allow Vivado Hardware Manager configuration and debug
- Fixed LVDS clock output to the Base board FPGA
- USB connection to the Base boards system monitor, to allow reporting of system monitor values

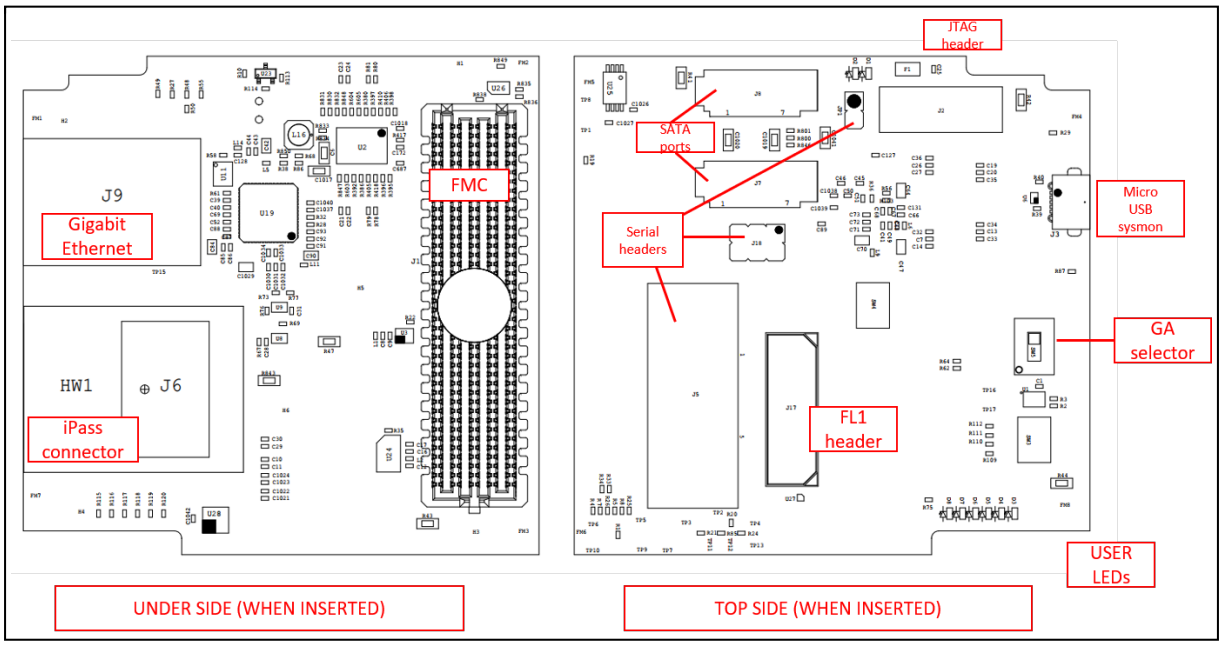

Figure 1 : ADM-SDEV-CFG2 Top and Bottom Views

1.2 References & Specifications

ANSI/VITA 57.1	*FPGA Mezzanine Card (FMC) Standard*, July 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 57.4	*FPGA Mezzanine Card Plus(FMC+) Standard*, March 2016, VITA, Draft

Table 1 : References

2 Installation

2.1 Software Installation

Please refer to the ADA-SDEV-KIT area on the Alpha-Data support site for access to system monitoring utilities, documentation and FPGA reference designs.

2.2 Hardware Installation

2.2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2.2 Configuration FMC Board

Prior to applying power to the ADM-SDEV-BASE board, the ADM-SDEV-CFG2 board should be fitted into the Config FMC Socket (J2).

it is recommended that the PMC keying pillar should be fitted to the ADM-SDEV-BASE board. This will ensure that only an ADM-SDEV-CFG1 can be fitted to the config FMC Socket.

Before powering on, adjust the GA selector switch depending on which generation of BASE board is being used. (See Below)

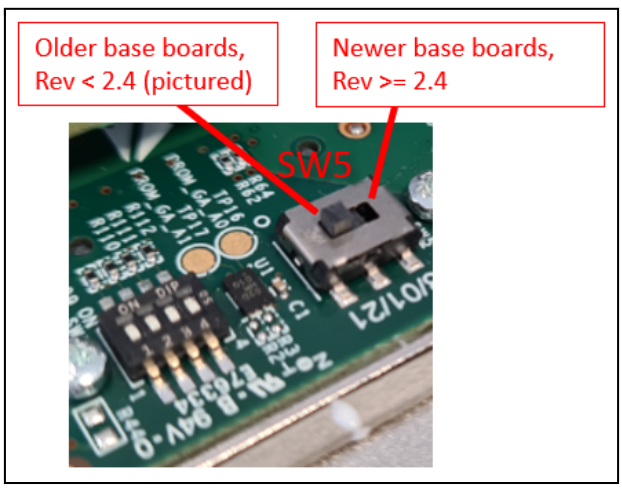

Figure 2 : Switch positions for different Base board revisions

3 Functional Description

3.1 Overview

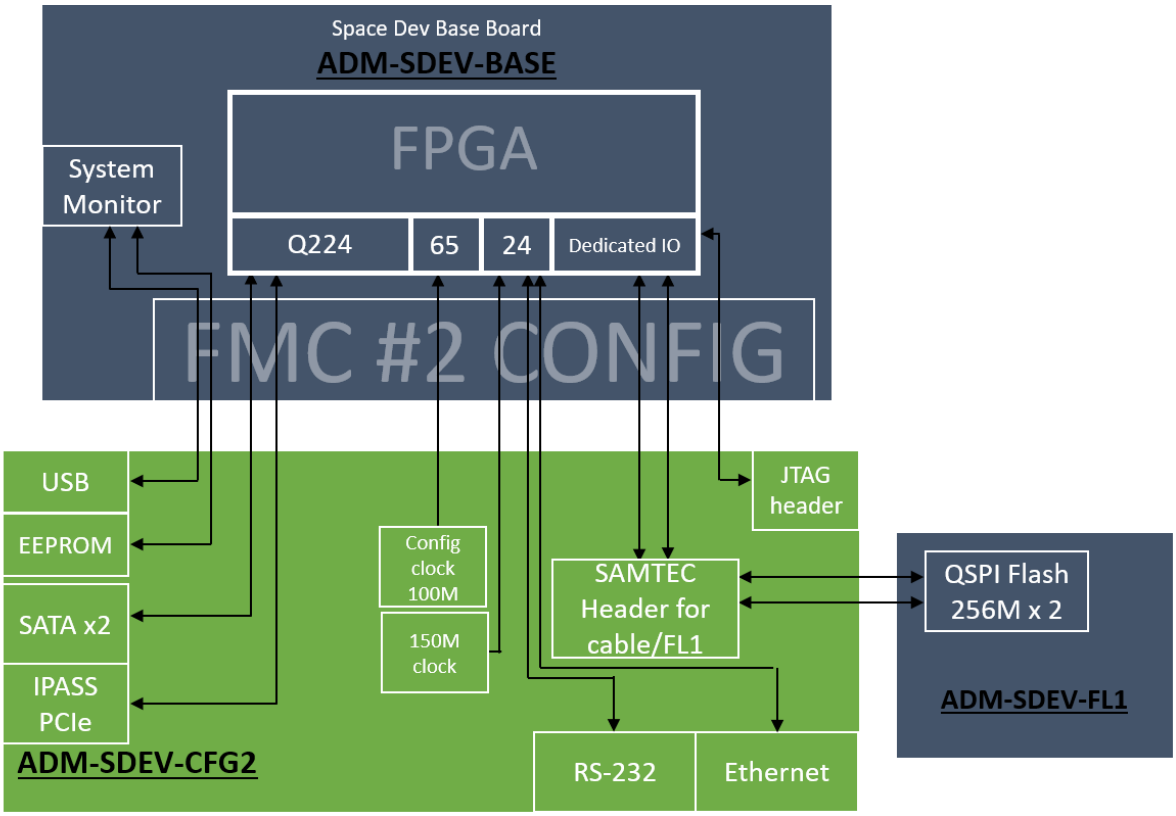

Figure 3 : ADM-SDEV-CFG1 Block Diagram

3.1.1 LED Definitions

The position and description of the board status LED is shown in LED Locations:

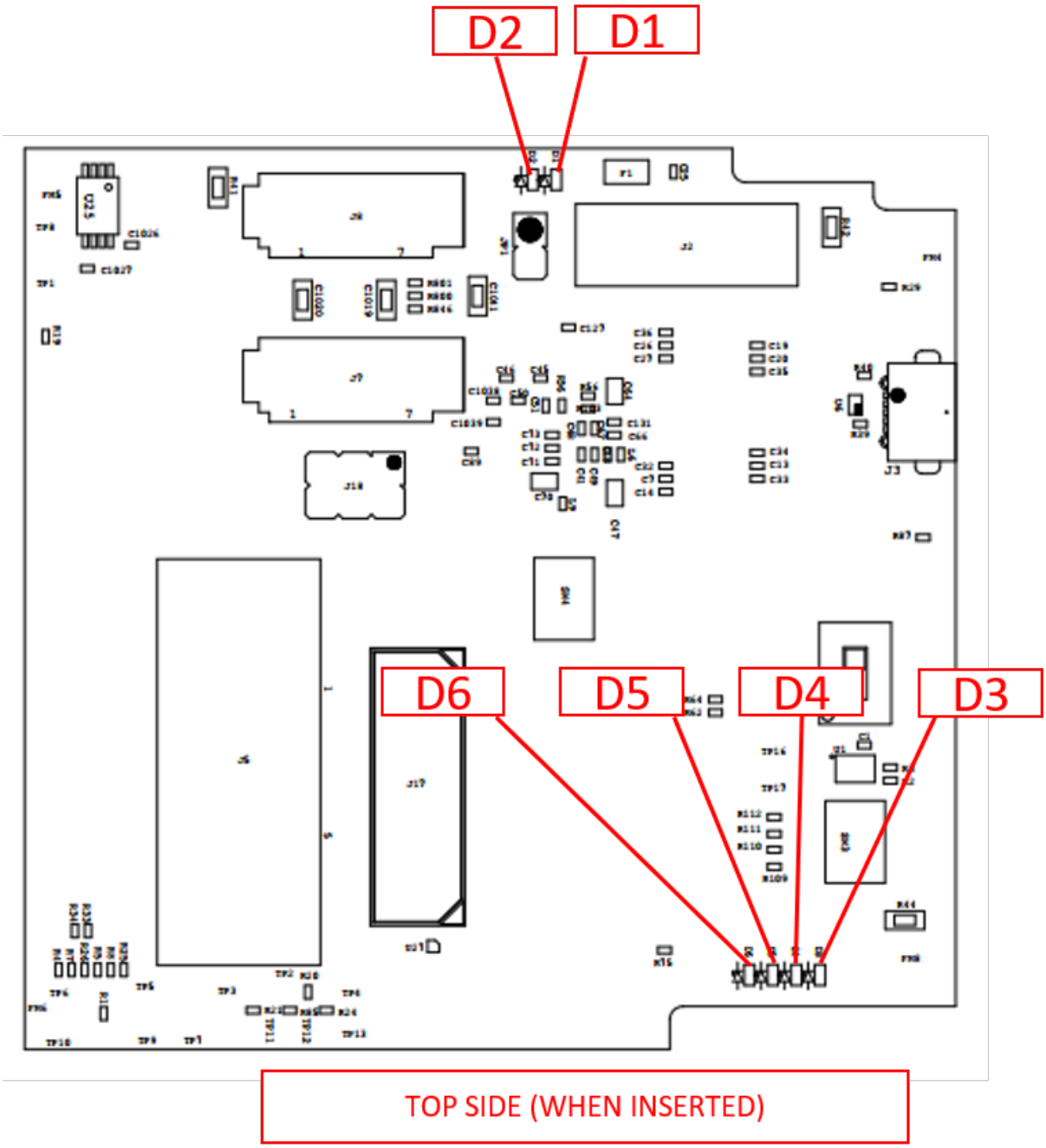

Figure 4 : LED Locations

Comp. Ref.	Function	ON State	Off State
D1(Green)	3.3V Supply Status	Normal operation	Power Off
D2(Green)	FMC VADJ Supply Status	Normal operation	Power Off
D3(Green)	User LED 0	User State	User State
D4(Green)	User LED 1	User State	User State
D5(Green)	User LED 2	User State	User State
D6(Green)	User LED 3	User State	User State

Table 2 : LED Definitions

3.2 Switches

3.2.1 Config mode switches: SW4

The FPGA Configuration mode switches M[2:0] are broken out onto the CFG2 board so the user can switch the FPGA configuration mode. See Xilinx Ultrascale Architecture Configuration guide UG570 for more information.

Comp. Ref.	Function
SW4_0	M[0]
SW4_1	M[1]
SW4_2	M[2]
SW4_3	N/C

Table 3 : User Switches

3.2.2 User Switches : SW3

The CFG2 board features four user switches which are connected to the Base board FPGA. The connections to the FPGA are shown below

Comp. Ref.	Function	FPGA pin
SW3_0	USER_SW_0	AK32
SW3_1	USER_SW_1	AL32
SW3_2	USER_SW_2	AJ31
SW3_3	USER_SW_3	AK31

Table 4 : User Switches

3.3 JTAG Interface

3.3.1 On-board Interface

The JTAG boundary scan chain can be accessed via a standard header (J2).

This allows the connection of the Xilinx JTAG cable for FPGA debug and QSPI Flash programming via the Xilinx toolchain.

The JTAG chain starts on the config FMC board and through the Base board, passing through the FPGA, the

LPC FMC (if fitted) and the FMC+ (if fitted).

The scan chain is shown in JTAG Boundary Scan Chain:

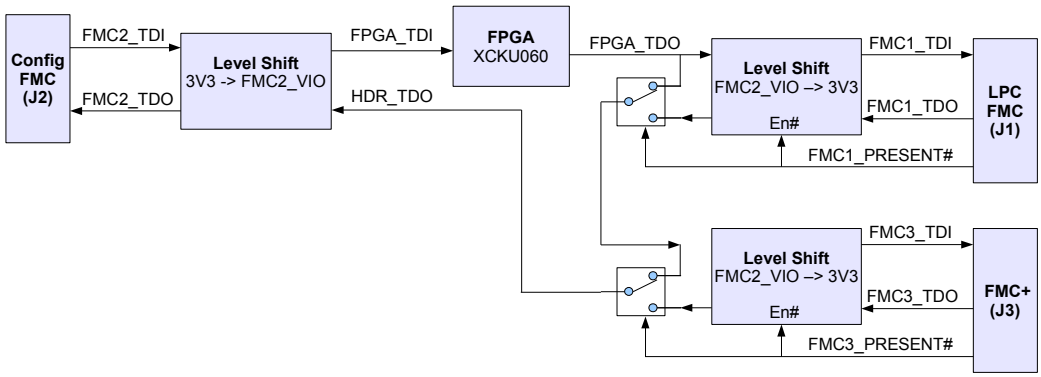

Figure 5 : JTAG Boundary Scan Chain

3.3.2 JTAG Voltages

The Vcc supply provided to the JTAG cable on the config header is +3.3V and is protected by a poly fuse rated at 375mA.

The voltage level of the JTAG chain on the ADM-SDEV-BASE board is set to the config FMC adjustable voltage FMC2_VIO.

3.4 Clocks

The **ADM-SDEV-CFG2** board can provides two different clock sources to the Base board FPGA.

One clock source is generated by an on board oscillator and the other can be input via connector J4.

Source	Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
Oscillator	CLK2_M2C_1	150MHz Fixed	Bank 24	LVDS	AM31	AN31
Oscillator	BPI_EMCCLK	100MHz Fixed	Bank 65	LVCMOS	AD14	N/A

Table 5 : Input CLK_M2C Connections

3.5 IPASS Connector

One of the high speed serial lanes is connected to an IPASS connector for remote PCIe connection.

Connector	Signal	FPGA Bank	"P" pin	"N" pin
IPASS (J6)	DP0_C2M	MGT Quad 224	AW8	AW7
	DP0_M2C	MGT Quad 224	AW4	AW3
	GBTCLK0_M2C	MGT Quad 224	AT10	AT9

Table 6 : IPASS PCIe Connections

3.6 SATA Connectors

The ADM-SDEV-CFG1 board has two standard right angle SATA receptacles for use with SATA compliant storage devices.

Connector	Signal	FPGA Bank	"P" pin	"N" pin
SATA_1 (J7)	DP2_C2M	MGT Quad 224	AU8	AU7
	DP2_M2C	MGT Quad 224	AU4	AU3
SATA_2 (J8)	DP3_C2M	MGT Quad 224	A16	A15
	DP3_M2C	MGT Quad 224	A12	A11

Table 7 : SATA Connections

3.7 Ethernet

There is a Gigabit Ethernet PHY on the CFG2, connected to the Base board using RGMII. There is an ethernet example design available from Alpha Data's website for this board

To	Signal	FPGA Bank	Pin
Ethernet PHY	RGMII_TXC	24	AM32
	RGMII_TX_CTL	24	AN32
	RGMII_TXD[0]	24	AJ30
	RGMII_TXD[1]	24	AK30
	RGMII_TXD[2]	24	AR31
	RGMII_TXD[3]	24	AR32
	RGMII_RXC	24	AL30
	RGMII_RX_CTL	24	AM30
	RGMII_RXD[0]	24	AJ33
	RGMII_RXD[1]	24	AK33
	RGMII_RXD[2]	24	AN33
	RGMII_RXD[3]	24	AP33
	MDIO	24	AU32
	MDC	24	AV32
	RST_N	24	AP30

Table 8 : Ethernet Connections to PHY

To ensure the correct operation of the LEDs on the ethernet jack, the LED configuration register inside the ethernet PHY must be set correctly. Failure to do so may affect the reliability of the PHY itself.

These register writes are performed in the example design.

The required writes are as follows:

Command	Address	Data	Function
Write	0x16	0x0003	Write Page Address 3
Write	0x11	0x442A	Set LED type to Open/Tristate
Write	0x16	0x0000	Write Page Address 0 (then resume other MDIO commands...)

Table 9 : Phy register writes

3.8 Serial Connections

There is a UART chip on the board, it has two channels, across 3 different pinout types. J5 and JP1 share transceiver 1, and J18 is connected to transceiver 2.

To	Signal	FPGA Bank	Pin
D-SUB (J5)	P1_COM1_TXD	24	AV19
	P1_COM1_RXD	24	AW18
2 Pin header (JP1)	P1_COM1_TXD	24	AV19
	P1_COM1_RXD	24	AW18
6 Pin header (J18)	P1_COM2_TXN	24	AT18
	P1_COM2_TXP	24	AT18
	P1_COM2_RXN	24	AT17
	P1_COM2_RXP	24	AT17

Table 10 : Serial Headers, and FPGA Connections to PHY

3.9 Configuration Flash and FL1 Daughter board

There is a config header on the board, A Samtec QSH-030-01-F-D-A-K. This is connected to the Base Board FPGA's SMAP and BPI configuration pins. By default, the CFG2 is supplied with the FL1 daugher board. This supplies two flash devices (MT25QU256ABA8E12-1SIT) to the FPGA Configuration pins which can be configured to hold an FPGA design using Vivado. The FPGA can boot from these flash devices.

The user may develop a custom breakout cable or board for these pins to meet their own configuration requirements. For the connector pinout, please see the CFG2 schematic

3.10 Health Monitoring

The **ADM-SDEV-BASE** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

The system monitor microcontroller can be accessed via the USB connector (J3), please refer to the ADM-SDEV-BASE user manual for more information.

3.11 GPIO Loopback

Many of the unused FMC GPIO signals are looped back on the ADM-SDEV-CFG2 board for test purposes.

Revision History

Date	Revision	Nature of Change
25 Mar 2021	0.1	Initial Draft
13 Apr 2021	0.2	More detail and images added
22 Apr 2021	1.0	Initial Release
27 Apr 2021	1.1	Updated GA Switch Image
27 Apr 2021	1.2	Removed Compatibility Table

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